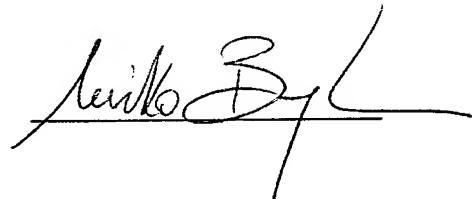


Express Mail No. EV529825025US

I, BERGADANO Mirko, an Italian citizen residing at  
10135 TORINO (Italy), Via Luigi Spazzapan, 16  
am acquainted with the Italian and English languages  
and certify that the attached is a true translation  
made by me into the English language of the certified  
copy relating to European Patent application No.  
00830148.3 filed on February 29, 2003.



Dated this 29<sup>th</sup> day of DECEMBER 2004



Europäisches  
Patentamt

European  
Patent Office

Office européen  
des brevets

Bescheinigung

Certificate

Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. Patent application No. Demande de brevet n°

00830148.3

Der Präsident des Europäischen Patentamts;  
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets  
p.o.

I.L.C. HATTEN-HECKMAN

DEN HAAG, DEN  
THE HAGUE,  
LA HAYE, LE  
15/02/01



Europäisches  
Patentamt

European  
Patent Office

Office européen  
des brevets

**Blatt 2 der Bescheinigung**  
**Sheet 2 of the certificate**  
**Page 2 de l'attestation**

Anmeldung Nr.: 00830148.3  
Application no.: 00830148.3  
Demande n°:

Anmeldetag:  
Date of filing: 29/02/00  
Date de dépôt:

Anmelder:  
Applicant(s):  
Demandeur(s):  
STMicroelectronics S.r.l.  
20041 Agrate Brianza (Milano)  
ITALY

Bezeichnung der Erfindung:  
Title of the Invention:  
Titre de l'invention:  
Process for forming a buried cavity in a semiconductor material wafer

**In Anspruch genommene Priorität(en) / Priority(ies) claimed / Priorité(s) revendiquée(s)**

Staat: Tag: Aktenzeichen:  
State: Date: File no.  
Pays: Date: Numéro de dépôt:

Internationale Patentklassifikation:  
International Patent classification:  
Classification internationale des brevets:  
H01L21/308

Am Anmeldetag benannte Vertragstaaten:  
Contracting states designated at date of filing: AT/BE/CH/CY/DE/DK/ES/FI/FR/GB/GR/IE/IT/LI/LU/MC/NL/PT/SE/ES  
Etats contractants désignés lors du dépôt:

Bemerkungen:  
Remarks:  
Remarques:

The original title of the application in Italian reads as follows:  
Procedimento di realizzazione di una cavità sepolta in una fetta  
di materiale semiconduttore.

PROCESS FOR FORMING A BURIED CAVITY IN A SEMICONDUCTOR  
MATERIAL WAFER

The present invention regards a process for forming  
5 a buried cavity in a semiconductor material wafer.

As is known, the possibility of manufacturing RF  
integrated circuits in CMOS or BiCMOS technology would  
make it possible to obtain lower consumption and lower  
costs as compared to normal circuits made using gallium  
10 arsenide (GaAs).

At present, however, this possibility is limited by  
the poor efficiency of the passive elements, and in  
particular by the inductors, on account of the high  
parasitic capacitances of the substrate which give rise  
15 to low resonance frequencies and preclude the use of  
high-frequency inductors, and on account of the high  
conductivity of the substrate, which markedly limits the  
quality factor  $Q$  of the inductor.

Typical values of the quality factor  $Q$  for  
20 integrated inductors made on GaAs are of the order of 20  
for frequencies of 2 GHz, whereas values of the quality  
factor  $Q$  smaller than 5 are obtained for inductors  
integrated on high-conductivity silicon substrates (CMOS  
processes).

25 To increase the quality factor  $Q$  of integrated  
inductors in the entire range of interest it is  
important to reduce both the losses due to the  
metallizations that make up the coil and losses due to

the substrate.

The losses due to metallizations can be reduced by using aluminium or copper thick layers having relatively high electrical conductivity. However, the skin effect, 5 which, for example, for copper is of the order of 1.5  $\mu\text{m}$  at a frequency of 1 GHz, limits the thickness of the metallization layer in which the current effectively flows. It follows therefore that there is no point in using metallization regions having a thickness of over 2 10  $\mu\text{m}$  to seek to increase the inductor quality factor  $Q$ .

The losses due to the substrate can be reduced by using high-resistivity substrates. However, this solution is not compatible with CMOS technology, which enables only low-resistivity substrates to be obtained.

15 One of the techniques used to reduce the losses due to the substrate envisages the formation of a thick oxide layer, namely of over 60  $\mu\text{m}$ , underneath the inductor, which limits the currents inductively generated in the substrate, thus improving the inductor 20 quality factor  $Q$  and at the same time enabling higher resonance frequencies to be obtained and wider metallization strips to be used, in this way also reducing ohmic dissipation.

25 This technique is schematically illustrated in Figures 1a-1c and envisages the formation, in a wafer 1 of monocrystalline silicon, of deep trenches 2 (Fig. 1a), complete thermal oxidation of the columns 3 of silicon comprised between each pair of contiguous

trenches 2 (Fig. 1b), and then chemical vapour deposition (CVD) of a layer of TEOS 4 (tetraethyl orthosilicate), the purpose of which is to complete filling of the trenches and to prepare the surface of 5 the substrate (planarization) for the subsequent forming of the inductor (Fig. 1c).

This technique is, however, very costly in that it requires a long time for forming the trenches (1  $\mu\text{m}/\text{min}$ ) and moreover with current etching machines it is not 10 possible to carry out the operation simultaneously on a number of wafers, but only on a single wafer at a time.

An alternative technique that has been proposed recently and that makes it possible to reduce losses due to the substrate is described in "PROCEEDINGS OF THE 15 IEEE", vol. 86, No. 8, August 1998, page 1632, and essentially envisages the creation of a cavity or air gap underneath the inductor by removing the silicon underneath the inductor by means of anisotropic chemical etches made using potassium hydroxide (KOH), tetramethyl 20 ammonium hydroxide (TMAH), etc., and employing a sacrificial polycrystalline-silicon layer.

This technique is schematically illustrated in Figures 2a-2c, and essentially involves the deposition and definition, using a special mask, of a sacrificial 25 polycrystalline-silicon layer 5 on the top surface of the substrate 1, deposition of a silicon-nitride (Si<sub>3</sub>N<sub>4</sub>) layer 6 above the sacrificial polycrystalline-silicon layer 5 (Fig. 2a), and then the carrying-out of an

anisotropic etch of the substrate 1 through an opening 7 made in the silicon-nitride layer 6 (Fig. 2b). By means of the anisotropic etch, the sacrificial polycrystalline-silicon layer 5 and part of the 5 substrate 1 are thus removed, and a cavity or air-gap 8 is obtained having a roughly triangular cross section, which is separated from the outside environment by a diaphragm 9 consisting of the portion of the silicon-nitride layer 6 overlying the cavity 8, and on which the 10 inductor can subsequently be made.

This technique presents some drawbacks that do not enable adequate exploitation of all its advantages.

In the first place, for the formation of the cavity 8 the above technique requires the deposition, and the 15 corresponding definition through a special mask, of a sacrificial polycrystalline-silicon layer 5, with the costs associated thereto.

In the second place, the said technique does not enable a uniform isolation level to be obtained 20 underneath the inductor, in that isolation is maximum at the centre of the cavity 8 (i.e., at the vertex that is set further down of the triangle) whilst it is minimum at the ends of the cavity 8 (i.e., at the two vertices of the triangle that are set higher up). Consequently, 25 in order to guarantee a minimum level of isolation of the inductor that may be acceptable over the entire extent of the latter, it is typically necessary to provide a cavity, the top area of which is larger than

the area of the inductor, with a consequent larger area occupied on the silicon with respect to the one that would be occupied if the known technique illustrated in Figures 1a-1c were instead used.

5        The object of the present invention is to provide a process for forming a buried cavity in a semiconductor material wafer that does not present the limitations of the processes of the known art.

10      According to the present invention, a process for forming a buried cavity in a semiconductor material wafer is provided, as defined in Claim 1.

15      For a better understanding of the present invention, preferred embodiments thereof are now described, merely to provide non-limiting examples, with reference to the attached drawings, in which:

      - Figures 1a-1c show cross sections of a semiconductor material wafer in successive steps of a first known forming process;

20      - Figures 2a-2c show cross sections of a semiconductor material wafer in successive steps of a second known forming process;

      - Figure 3 shows a top view of a semiconductor material wafer in which the cavity has a pre-set orientation with respect to the wafer;

25      - Figures 4a-4d show cross sections of the wafer of Figure 3 at an enlarged scale in successive forming steps, according to the present invention;

      - Figures 5 and 6 show portions of masks used

during the forming process according to the present invention; and

- Figures 7a and 7b show cross sections of the wafer of Figure 4d in successive forming steps,  
5 according to a different embodiment of the invention.

Figure 3 shows a wafer in which a cavity or air gap 20 is formed using a holed mask 16 having openings oriented at approximately 45° with respect to the "flat" of the wafer 10, identified by the orientation <110>, as 10 is shown in the detail of Figure 5. The surface of the wafer 10 has, instead, orientation <100>.

For forming the cavity 20, according to what is illustrated in Figures 4a-4d, directly on the top surface 13 of a P or P+ monocrystalline silicon 15 substrate 11 (i.e., without the interposition of a sacrificial polycrystalline-silicon layer), a first silicon-dioxide layer 12 is initially grown having a thickness of between 200 Å and 600 Å, and a silicon-nitride layer 14 is next deposited thereon having a 20 thickness of between 900 and 1500 Å (Fig. 4a).

Next, using a resist mask (not shown), dry etching is carried out of the uncovered portions of the silicon-nitride layer 14 and of the silicon-dioxide layer 12, and the resist mask is then removed. In this way, the 25 portions of the silicon-nitride layer 14 and of the silicon-dioxide layer 12 that have remained after the dry etching form the holed mask 16 (Fig. 4b).

As is illustrated in detail in Figure 5, the holed

mask 16 has a lattice structure provided with openings 18 having a substantially square cross section, with sides having a length L1 of, for example, between 1  $\mu\text{m}$  and 3  $\mu\text{m}$ , preferably 2  $\mu\text{m}$ , and an inclination of  $45^\circ \pm 1^\circ$  5 with respect to the "flat" of the wafer 10. The openings are set apart at a distance comparable to the length L1, and hence, for example, at a distance of between 1  $\mu\text{m}$  and 3  $\mu\text{m}$ .

Using the holed mask 16, the substrate 11 is then 10 anisotropically etched under time control in tetramethyl ammonium hydroxide (TMAH), thus forming the cavity 20, which substantially has the shape of an isosceles trapezium turned upside down and a depth of between 50  $\mu\text{m}$  and 100  $\mu\text{m}$  (Fig. 4c).

15 In particular, the shape of an upside-down isosceles trapezium of the cavity 20 is obtained thanks to the combination of the following factors: execution of an anisotropic etch; use of a holed mask 16; and orientation at  $45^\circ \pm 1^\circ$  of the openings 18 with respect 20 to the "flat" of the wafer 10.

In fact, with the particular combination described above, the individual etches having their origin from the openings 18 of the holed mask 16 are performed on particular crystallographic planes of the silicon which 25 enable the individual etches to "join up" laterally to one another, thus causing removal of the silicon not only in the vertical direction (i.e., in the direction of the depth of the substrate 11), but also in the

horizontal direction (width/length), thus leading to the formation of the cavity 20 having the shape shown in Figure 4c.

If, instead, the openings 18 of the holed mask 16 5 had sides parallel or orthogonal to the "flat" of the wafer 10, the individual etches having their origin from the opening 18 of the holed mask 16 would be performed on crystallographic planes of the silicon that would not enable the individual etches to "join up" laterally to 10 one another, thus leading to the formation of a set of cavities, equal in number to the openings 18 of the holed mask 16, separate from one another, and each having a cross section shaped like an upside-down triangle, of the same type as that shown in Figure 2c.

15 The use of TMAH for carrying out anisotropic etching of the substrate 11 is moreover particularly advantageous in combination with the structure of the holed mask 16 described above for leading to the formation of the cavity 20 having the shape illustrated 20 in Figure 4c, in that also this contributes to lateral joining-up of the individual etches.

With reference again to Figures 4a-4d, following upon TMAH anisotropic etching, a chemical vapour deposition (CVD) of tetraethyl orthosilicate (TEOS) is 25 carried out for a thickness of 2  $\mu\text{m}$ , which leads to the formation of a coating layer 22, which is thinner and which coats the side walls and bottom wall of the cavity 20, and of a closing layer 24 which completely closes

the openings of the holed mask 16 (Fig. 4d).

The closing layer 24 defines, on top of the cavity 20, a diaphragm 26, above which, in a way in itself known and not illustrated, the suspended structure can 5 then made, such as an inductor, a resistor, etc.

The advantages of the process according to the present invention are described in what follows.

In the first place, forming cavities according to the present invention does not entail the deposition, 10 and the corresponding definition through a dedicated mask, of a special polycrystalline-silicon layer; the fabrication process is consequently simpler and more economical, thanks to the reduction in the number of the steps required, and in particular to the elimination of 15 the mask necessary for the definition of the sacrificial polycrystalline-silicon layer.

In the second place, the process described enables the fabrication of a cavity 20 the shape of which makes it possible to achieve a uniform isolation level beneath 20 the electronic component (inductor, resistor, etc.) made on the diaphragm 26 overlying the cavity 20, thus reducing occupation of the area on silicon with respect to that which there would be if the prior art techniques shown in Figures 2a-2c were used.

25 In addition, the present process can be employed for the formation of cavities having, in plan view, any shape whatsoever, and even elongated cavities defining true buried channels.

Finally, it is clear that numerous modifications and variations can be made to the process described and illustrated herein, without thereby departing from the sphere of protection of the present invention, as 5 defined in the attached claims.

For example, the holed mask used in the process could also present a different pattern of the openings. For instance, it is possible to use the pattern shown in Figure 6, in which the holed mask 16' has openings 18' 10 having a substantially rectangular shape, with the smaller side having a length L1 of, for example, between 1  $\mu\text{m}$  and 3  $\mu\text{m}$ , preferably 2  $\mu\text{m}$ , and the larger side having a length L2 of, for example, between 1  $\mu\text{m}$  and 10  $\mu\text{m}$ , preferably 5-7  $\mu\text{m}$ , and an inclination of  $45^\circ \pm 1^\circ$  15 with respect to the "flat" of the wafer 10. The distance between the openings 18' is preferably comparable with that of the smaller side L1, and is hence, for example, between 1  $\mu\text{m}$  and 3  $\mu\text{m}$ .

In addition, the openings 18' are arranged in 20 parallel rows, and the openings 18' belonging to adjacent rows are staggered with respect to one another.

Furthermore, the openings 18' could present a shape slightly different from that illustrated in Figure 6. In particular, they could present any shape elongated along 25 a prevalent direction having the inclination referred to above with respect to the "flat" of the wafer 10, for example the shape of a flattened ellipse, a generally quadrangular elongated shape, etc.

Finally, the same process can be used to make buried channels connected with the outside world at communication openings, for example elongated channels having two opposite ends and being connected via 5 communication openings set at the ends of the channels themselves. In this case, the openings 18, 18' of the holed mask 16, 16' are arranged so as to obtain the desired shape for the cavity 20 or for a plurality of cavities 20. In addition, instead of depositing TEOS 10 after the formation of the cavity 20, polycrystalline silicon is deposited, which comes to form the coating layer 22 and the closing layer 24. Next, as shown in Figure 4a, an epitaxial layer 30 is grown so as to strengthen the diaphragm 26. Finally, using known 15 etching techniques, the openings 31 are made at the two ends of the cavity or of each cavity 20 (Figure 7b), so as to form areas of access to the cavity or cavities 20. This solution is particularly suited for the fabrication of microreactors for the DNA chain reaction.

CLAIMS

1. A process for forming a buried cavity (20) in a semiconductor material body (11), comprising the steps of:

5       - forming a mask (16) on top of said semiconductor material body (11); and

      - anisotropically etching said semiconductor material body (11) using said mask (16);

10       characterized in that said mask (16) has a plurality of openings (18; 18'), each having a side or a prevalent direction with an inclination of between 44° and 46° with respect to a flat (100) of said semiconductor material body (11).

15       2. The process according to Claim 1, characterized in that said openings (18) have a side or a prevalent direction with an inclination of 45° with respect to said flat (100) of said semiconductor material body (11).

20       3. The process according to Claim 1 or Claim 2, characterized in that said openings (18; 18') have a quadrangular shape.

      4. The process according to Claim 3, characterized in that said openings (18) have a substantially square shape.

25       5. The process according to Claim 3, characterized in that said openings (18') have a substantially rectangular shape.

      6. The process according to Claim 5, characterized in

that said openings (18') are arranged in parallel rows.

7. The process according to Claim 6, characterized in that said openings (18') belonging to adjacent rows are staggered with respect to one another.

5 8. The process according to any of the foregoing claims, characterized in that said mask (16) has a lattice structure.

9. The process according to any of the foregoing claims, characterized in that said mask (16) is made 10 directly above a surface (13) of said semiconductor material body (11).

10. The process according to any of the foregoing claims, characterized in that said anisotropic etching step is carried out using TMAH.

15 11. The process according to any of the foregoing claims, characterized in that said anisotropic etching step is time-controlled.

12. The process according to any of the foregoing claims, characterized by the further step of:

20 - forming, above said mask (16), a coating layer (22) closing said openings (18; 18').

13. The process according to Claim 12, characterized in that said step of forming a coating layer (22) comprises carrying out TEOS chemical vapour deposition.

25 14. The process according to Claim 12, characterized in that said step of forming a coating layer (22) comprises the deposition of a polycrystalline-silicon layer.

15. The process according to Claim 13,  
characterized by the further steps of growing an  
epitaxial layer (30) on said coating layer and of  
forming communication openings (31) extending in said  
5 epitaxial layer (31) and in said coating layer as far as  
said cavity (20).

16. The process according to any of the foregoing  
claims, characterized in that said mask (16) is a hard  
mask comprising oxide portions (12) in contact with said  
10 semiconductor material body (11) and silicon-nitride  
portions (14) above said oxide portions (12).

ABSTRACT

The process comprises the steps of forming, on top of a semiconductor material wafer (10), a holed mask (16) having a lattice structure and comprising a plurality of 5 openings (18) each having a substantially square shape and a side with an inclination of 45° with respect to the flat (100) of the wafer; carrying out an anisotropic etch in TMAH of the wafer (10), using said holed mask (16), thus forming a cavity (20), the cross section of 10 which has the shape of an upside-down isosceles trapezium; and carrying out a chemical vapour deposition (CVD) using TEOS, thus forming a TEOS layer (24) which completely closes the openings of the holed mask (16) and defines a diaphragm (26) overlying the cavity (20) 15 and on which a suspended integrated structure can subsequently be manufactured.

Figures 4c, 4d, 5